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PATENT & TRADEMARK OFFICE

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re PATENT application of:

Hiroshige HIRANO et al.

Art Unit: 2814

Application No.: 09/333,049

Examiner: Hoai PHAM

Filed: June 15, 1999

For: FERROELECTRIC MEMORY DEVICE

TECHNOLOGY CENTER 2800
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AMENDMENT UNDER 37 C.F.R. 1.111

Commissioner of Patents
Washington, D.C. 20231

November 26, 2001
(Monday)

Dear Sir:

In response to the Examiner's non-Final Office Action mailed July 24, 2001, please consider the following amendments and remarks in connection with the above-identified application.

IN THE CLAIMS:

Please amend claims 1, 8, and 9 to read as follows:

Subd C1

1. (Thrice Amended) A ferroelectric memory device comprising:

a ferroelectric capacitor including a top electrode, a bottom electrode and a ferroelectric film interposed between the top and bottom electrodes, the top electrode having a rectangular planar pattern;

a memory cell transistor including first and second doped layers and a gate, the memory cell transistor controlling a voltage supplied to the top electrode of the ferroelectric capacitor;

an interlevel dielectric film formed over the memory cell transistor and the ferroelectric capacitor;

a first interconnection layer formed on the interlevel dielectric film